Devadarsh A Nair

B.E. (Hons.) Electronics and Electrical Engineering, BITS Pilani K.K. Birla Goa Campus
devadarsh.nair@gmail.com · f20240330@goa.bits-pilani.ac.in · +91 9148465240
devnair.me · github.com/devadarshnair · Goa, India

Education

BITS Pilani, K.K. Birla Goa Campus — Goa, India
B.E. (Hons.) Electronics and Electrical Engineering *CGPA: 8.91 / 10* — *2024 – 2028*

DEENS Academy, Bangalore *Class XII, CBSE: 92.8%* — *2023*

Delhi Public School, East, Bangalore *Class X, CBSE: 94.16%* — *2021*

Experience

CircuitEvolve — Research Intern
Analog circuit optimization using evolutionary learning algorithms — *May 2026 – July 2026*

- Built the LLM-guided evolutionary optimizer at the core of the company's analog design automation flow: parallel subagents propose, mutate, and critique candidate topologies, a fitness pipeline scores them against target specifications, and every survivor is verified in SPICE before entering the next generation.
- Lead a research section on yield-informed circuit reasoning, extending the optimizer beyond nominal specifications so that search decisions account for process variation, device mismatch, and expected yield, keeping generated circuits robust across PVT corners.
- Part of the technical team preparing a conference paper submission on the framework; own the experimental evaluation and benchmarking against baseline sizing and topology-search methods.

Projects

Efficient Long-Context Transformers & Parameter-Efficient Fine-Tuning — SAiDL
Independent research project — *April 2026 – June 2026*

- Developed a modular decoder-only transformer framework with swappable attention, positional encodings, and block structures; benchmarked six attention variants (standard, sliding-window, sparse-block, linear, GQA, MQA) on perplexity, peak VRAM, and throughput across context lengths 256 to 4096 on a single RTX 4060.
- Ran a train-short-test-long extrapolation study across five positional encodings (learned, sinusoidal, RoPE, ALiBi, relative bias) and evaluated causal convolution-attention hybrid blocks.
- Compared LoRA, AdaLoRA, and SoRA on GLUE CoLA; implemented the proximal soft-thresholding update from scratch in NumPy and PyTorch, verified it against the L1 subgradient alternative, and extended the SoRA sparsity principle to xLSTM and Mamba backbones.

RV32I 5-Stage Pipelined RISC-V Processor — BITSilicon
Project Lead, 12-member team — *May 2026 – Present*

- Leading the design of a fully synthesizable 32-bit RISC-V processor in Verilog: a 5-stage in-order pipeline with full forwarding, stall insertion, static branch prediction, and Harvard memory interfaces, synthesized for a Xilinx Artix-7 FPGA.
- Own the microarchitecture decisions, task allocation, and integration across RTL, verification, and synthesis workstreams; the design is being submitted to a tape-out competition with a path to silicon fabrication.
- Roadmap targets high-performance compute extensions (caches, memory hierarchy, performance counters) for studying data-movement bottlenecks in compute-intensive and AI-adjacent workloads.

Technical Skills

ML & Research Frameworks	PyTorch (CUDA), Hugging Face Transformers, Datasets, PEFT, Accelerate, scikit-learn, NumPy, SciPy, pandas, einops
Experiment Tooling	Weights & Biases, Hydra/OmegaConf configs, pytest, matplotlib, Git, LaTeX
LLM & Agent Systems	LLM APIs (Anthropic, OpenAI), multi-agent and subagent orchestration, LLM-guided evolutionary search, evaluation-harness and prompt design, agentic coding workflows
Hardware & EDA	Verilog, Verilator, Icarus Verilog, GTKWave, Sentaurus TCAD, Cadence Virtuoso, LTspice, Proteus, Simulink
Programming	Python, C, C++, MATLAB, x86 Assembly (MASM)

Achievements

- **Samsung Semiconductor Research Fellow, ISWDP Cohort 7 (IISc Bangalore)**: awarded the merit-based Samsung fellowship of the India Semiconductor Workforce Development Program, an IISc program run with Samsung Semiconductor India Research and Synopsys to build advanced device-design and process-technology talent.
- **Invited Attendee, Synopsys Users Group (SNUG) India 2026**: participated on direct invitation in Synopsys' flagship technical conference, an event restricted to Synopsys partner organizations and their invitees.